L Number	Hits	Search Text	DB	Time stamp
1	0	silicon and (germanium with "%") and (threading adj dislocation)	EPO; JPO; DERWENT; IBM_TDB	2004/09/23 15:31
2	5	silicon and (germanium with "%") and (threading adj dislocation)	USPAT; US-PGPUB	2004/09/23 15:34
3	24	silicon and (Ge with "%") and (threading adj dislocation)	USPAT; US-PGPUB	2004/09/23 15:44
4	22	(silicon and (Ge with "%") and (threading adj dislocation)) not (silicon and (germanium with "%") and (threading adj dislocation))	USPAT; US-PGPUB	2004/09/23 15:35
5	13	((silicon and (Ge with "%") and (threading adj dislocation)) not (silicon and (germanium with "%") and (threading adj dislocation))) and @ad<20020823	USPAT; US-PGPUB	2004/09/23 15:35
6	0	silicon and (Ge with "%") and (threading adj dislocation)	EPO; JPO; DERWENT; IBM_TDB	2004/09/23 15:44

L Number	Hits	Search Text	DB	Time stamp
6	3	(hetero adj (structure or junction)) and silicon and (germanium with graded)	USPAT; US-PGPUB	2004/09/23 13:56
7	1996	silicon and germanium and graded	USPAT; US-PGPUB	2004/09/23 13:56
8	238	silicon and (germanium with graded)	USPAT; US-PGPUB	2004/09/23 14:11
9	173	(silicon and (germanium with graded)) and (epitaxial$2)	USPAT; US-PGPUB	2004/09/23 13:56
10	127	((silicon and (germanium with graded)) and (epitaxial$2)) and @ad<20020823	USPAT; US-PGPUB	2004/09/23 13:58
11	41	(((silicon and (germanium with graded)) and (epitaxial$2)) and @ad<20020823) and dislocation	USPAT; US-PGPUB	2004/09/23 14:12
12	35	((((silicon and (germanium with graded)) and (epitaxial$2)) and @ad<20020823) and dislocation) and density	USPAT; US-PGPUB	2004/09/23 13:58
13	30	((((silicon and (germanium with graded)) and (epitaxial$2)) and @ad<20020823) and dislocation) and (dislocation with density)	USPAT; US-PGPUB	2004/09/23 13:59
14	45	silicon and (germanium with graded)	EPO; JPO; DERWENT; IBM_TDB	2004/09/23 14:12
15	7	(silicon and (germanium with graded)) and dislocation	EPO; JPO; DERWENT; IBM_TDB	2004/09/23 14:12

PUB-NO: EP000514018A2

DOCUMENT-IDENTIFIER: EP 514018 A2

TITLE: Method for making low defect density semiconductor heterostructure and devices made thereby.

PUBN-DATE: November 19, 1992

INVENTOR-INFORMATION:

NAME	COUNTRY
BRASEN, DANIEL	US
FITZGERALD, EUGENE ARTHUR JR	US
GREEN, MARTIN LAURENCE	US
XIE, YA-HONG	US

ASSIGNEE-INFORMATION:

NAME	COUNTRY
AMERICAN TELEPHONE & TELEGRAPH	US

APPL-NO: EP92303475

APPL-DATE: April 16, 1992

PRIORITY-DATA: US69042991A (April 24, 1991)

INT-CL (IPC): H01L021/20, H01L021/335 , H01L033/00

EUR-CL (EPC): H01L021/335 ; H01L027/15, H01L033/00 , H01L033/00 , H01L021/20 , H01L021/8258

US-CL-CURRENT: 117/89, 117/105 , 117/108

ABSTRACT:

<CHG DATE=19950204 STATUS=O> Applicants have discovered that by growing

germanium-silicon alloy at high temperatures in excess of about 850 DEG C and increasing the **germanium** content at a gradient of less than about 25% per micrometer, one can grow on **silicon** large area heterostructures of **graded** GexSi1-x alloy having a low level of threading **dislocation** defects. With low concentrations of germanium (.10</= x </=.50), the heterolayer can be used as a substrate for growing strained layer **silicon** devices such as MODFETS. With high concentrations of Ge (.65 </= x </= 1.00) the heterolayer can be used on **silicon** substrates as a buffer layer for indium gallium phosphide devices such as light emitting diodes and lasers. At concentrations of pure germanium (X=1.00), the heterolayer can be used for GaAs or GaAs/AlGaAs devices. <IMAGE>

DERWENT-ACC-NO: 2002-241247

DERWENT-WEEK: 200402

TITLE: Monocrystalline etch-stop layer system for use on monocrystalline **silicon** substrate, comprises relaxed **graded** layer of **silicon-germanium**

INVENTOR: BORENSTEIN, J T; FITZGERALD, E A ; TARASCHI, G ; WU, K C

PATENT-ASSIGNEE: MASSACHUSETTS INST TECHNOLOGY[MASI]

PRIORITY-DATA: 2000US-0599260 (June 22, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 200199169 A2	December 27, 2001	E	048	H01L 021/306
AU 200168577 A	January 2, 2002	N/A	000	H01L 021/306
EP 1295319 A2	March 26, 2003	E	000	H01L 021/306
JP 2003536273 W	December 2, 2003	N/A	064	H01L 021/306

DESIGNATED-STATES: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI
GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG
MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD
SE SL SZ TR TZ UG ZW AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC
MK NL PT RO SE SI TR

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO

	APPL-DATE	
WO 200199169A2	N/A	
2001WO-US19613	June 20, 2001	
AU 200168577A	N/A	
2001AU-0068577	June 20, 2001	
AU 200168577A	Based on	WO 200199169 N/A
EP 1295319A2	N/A	
2001EP-0946546	June 20, 2001	
EP 1295319A2	N/A	
2001WO-US19613	June 20, 2001	
EP 1295319A2	Based on	WO 200199169 N/A
JP2003536273W	N/A	
2001WO-US19613	June 20, 2001	
JP2003536273W	N/A	
2002JP-0503924	June 20, 2001	
JP2003536273W	Based on	WO 200199169 N/A

INT-CL (IPC): B81C001/00, H01L021/306 , H01L029/165

RELATED-ACC-NO: 1999-611440

ABSTRACTED-PUB-NO: WO 200199169A

BASIC-ABSTRACT:

NOVELTY - A monocrystalline etch-stop layer system comprises a relaxed **graded** layer of **silicon-germanium** and a uniform etch-stop layer of relaxed **silicon-germanium**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of integrating a device or layer by:

(i) depositing a relaxed **graded** layer of **silicon-germanium on a silicon** substrate;

(ii) depositing a uniform etch-stop layer of relaxed **silicon-germanium on the graded** buffer; and

(iii) etching portions of the substrate and the graded

buffer to release the
etch-stop layer.

USE - For use on monocrystalline **silicon** substrate.

ADVANTAGE - The use of a graded layer suppresses the threading **dislocation**
density (TDD) in the top etch-stop layer, which leads to a uniform, nearly
defect-free Si1-xGex etch stop.

CHOSEN-DRAWING: Dwg.0/15

TITLE-TERMS: MONOCRYSTAL ETCH STOP LAYER SYSTEM MONOCRYSTAL **SILICON** SUBSTRATE
COMPRISE RELAX GRADE LAYER **SILICON** GERMANIUM

DERWENT-CLASS: L03 Q68 U11

CPI-CODES: L04-A01C; L04-C07;

EPI-CODES: U11-C01J4A; U11-C05B9A;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2002-072471
Non-CPI Secondary Accession Numbers: N2002-186348

DERWENT-ACC-NO: 1999-081518

DERWENT-WEEK: 200437

TITLE: Use of **graded germanium-silicon** layers for mismatched layers - on a **silicon** substrate, enabling the threading **dislocation** density to be controlled

INVENTOR: FITZGERALD, E A

PATENT-ASSIGNEE: MASSACHUSETTS INST TECHNOLOGY[MASI] , FITZGERALD E A[FITZI]

PRIORITY-DATA: 1997US-059765P (September 16, 1997) , 1997US-050602P (June 24, 1997) , 1998US-0103672 (June 23, 1998) , 1999US-0265016 (March 9, 1999) , 2000US-0712604 (November 14, 2000) , 2001US-0022689 (December 17, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC	
JP 3535527 B2	June 7, 2004		011	H01L 021/20	N/A
WO 9859365 A1	December 30, 1998		023	H01L 021/20	E
EP 1016129 A1	July 5, 2000		000	H01L 021/20	E
US 6107653 A	August 22, 2000		000	H01L 031/0256	N/A
JP 2000513507 W	October 10, 2000		023		N/A
KR 2001014201 A	February 26, 2001		000	H01L 021/20	N/A
US 6291321 B1	September 18, 2001		000	H01L 021/20	N/A
US 20020084000 A1	July 4, 2002		000	H01L 021/20	N/A
KR 400808 B	October 8, 2003		000	H01L 021/36	N/A

H01L 021/20

DESIGNATED-STATES: CA JP KR AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT
SE AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 3535527B2	N/A		
1998WO-US13076	June 23, 1998		
JP 3535527B2	N/A		
1999JP-0505004	June 23, 1998		
JP 3535527B2	Previous Publ.	JP 200013507	N/A
JP 3535527B2	Based on	WO 9859365	N/A
WO 9859365A1	N/A		
1998WO-US13076	June 23, 1998		
EP 1016129A1	N/A		
1998EP-0931529	June 23, 1998		
EP 1016129A1	N/A		
1998WO-US13076	June 23, 1998		
EP 1016129A1	Based on	WO 9859365	N/A
US 6107653A	Provisional		
1997US-050602P	June 24, 1997		
US 6107653A	Provisional		
1997US-059765P	September 16, 1997		
US 6107653A	N/A		
1998US-0103672	June 23, 1998		
JP2000513507W	N/A		
1998WO-US13076	June 23, 1998		
JP2000513507W	N/A		
1999JP-0505004	June 23, 1998		
JP2000513507W	Based on	WO 9859365	N/A
KR2001014201A	N/A		
1999KR-0712279	December 24, 1999		
US 6291321B1	Provisional		
1997US-050602P	June 24, 1997		
US 6291321B1	Provisional		
1997US-059765P	September 16, 1997		
US 6291321B1	Div ex		
1998US-0103672	June 23, 1998		
US 6291321B1	N/A		
1999US-0265016	March 9, 1999		

US 6291321B1	Div ex	US 6107653
N/A		
US20020084000A1	Provisional	
1997US-050602P	June 24, 1997	
US20020084000A1	Provisional	
1997US-059765P	September 16, 1997	
US20020084000A1	Div ex	
1998US-0103672	June 23, 1998	
US20020084000A1	Cont of	
1999US-0265016	March 9, 1999	
US20020084000A1	Cont of	
2000US-0712604	November 14, 2000	
US20020084000A1	N/A	
2001US-0022689	December 17, 2001	
US20020084000A1	Div ex	US 6107653
N/A		
US20020084000A1	Cont of	US 6291321
N/A		
KR 400808B	N/A	
1998WO-US13076	June 23, 1998	
KR 400808B	N/A	
1999KR-0712279	December 24, 1999	
KR 400808B	Previous Publ.	KR2001014201
N/A		
KR 400808B	Based on	WO 9859365
N/A		

INT-CL (IPC): C30B001/00, H01L021/20 , H01L021/36 , H01L029/04 , H01L029/12 , H01L029/30 , H01L031/0256 , H01L031/36

ABSTRACTED-PUB-NO: US 6107653A

BASIC-ABSTRACT:

A semiconductor structure comprises: a) a semiconductor substrate; b) at least one first crystalline epitaxial layer, having a planarised surface, on the semiconductor substrate; and c) at least one second crystalline epitaxial layer on the first crystalline epitaxial layer. More specifically, the semiconductor structure comprises a Si substrate on which is grown a GeSi graded region. The graded region incorporates compressive strain to offset the tensile strain that

is incorporated during thermal processing.

Also claimed is a method of fabricating a semiconductor structure as above.

USE - Useful in the fabrication of semiconductor devices, especially III-V
devices on a Si substrate.

ADVANTAGE - Allows controlled relaxation of mix-matched semiconductor layers.
Provides for a chemical-mechanical planarisation method in conjunction with the
growth of relaxed graded buffers to 100% Ge without a concomitant increase in
threading **dislocation** density. Provides modifications to UHV-CVD procedures
which eliminate surface cracks due to the thermal mismatch between Si and Ge,
and particulate defects due to gas-phase nucleation.

ABSTRACTED-PUB-NO: US 6291321B

EQUIVALENT-ABSTRACTS:

A semiconductor structure comprises: a) a semiconductor substrate; b) at least
one first crystalline epitaxial layer, having a planarised surface, on the
semiconductor substrate; and c) at least one second crystalline epitaxial layer
on the first crystalline epitaxial layer. More specifically, the semiconductor
structure comprises a Si substrate on which is grown a GeSi graded region. The
graded region incorporates compressive strain to offset the tensile strain that
is incorporated during thermal processing.

Also claimed is a method of fabricating a semiconductor structure as above.

USE - Useful in the fabrication of semiconductor devices, especially III-V
devices on a Si substrate.

ADVANTAGE - Allows controlled relaxation of mix-matched semiconductor layers.

Provides for a chemical-mechanical planarisation method in conjunction with the growth of relaxed graded buffers to 100% Ge without a concomitant increase in threading **dislocation** density. Provides modifications to UHV-CVD procedures which eliminate surface cracks due to the thermal mismatch between Si and Ge, and particulate defects due to gas-phase nucleation.

A semiconductor structure comprises: a) a semiconductor substrate; b) at least one first crystalline epitaxial layer, having a planarised surface, on the semiconductor substrate; and c) at least one second crystalline epitaxial layer on the first crystalline epitaxial layer. More specifically, the semiconductor structure comprises a Si substrate on which is grown a GeSi graded region. The graded region incorporates compressive strain to offset the tensile strain that is incorporated during thermal processing.

Also claimed is a method of fabricating a semiconductor structure as above.

USE - Useful in the fabrication of semiconductor devices, especially III-V devices on a Si substrate.

ADVANTAGE - Allows controlled relaxation of mix-matched semiconductor layers.

Provides for a chemical-mechanical planarisation method in conjunction with the growth of relaxed graded buffers to 100% Ge without a concomitant increase in threading **dislocation** density. Provides modifications to UHV-CVD procedures which eliminate surface cracks due to the thermal mismatch between Si and Ge, and particulate defects due to gas-phase nucleation.

US20020084000A

A semiconductor structure comprises: a) a semiconductor substrate; b) at least one first crystalline epitaxial layer, having a planarised

surface, on the
semiconductor substrate; and c) at least one second crystalline epitaxial layer
on the first crystalline epitaxial layer. More specifically, the semiconductor
structure comprises a Si substrate on which is grown a GeSi graded region. The
graded region incorporates compressive strain to offset the tensile strain that
is incorporated during thermal processing.

Also claimed is a method of fabricating a semiconductor structure as above.

USE - Useful in the fabrication of semiconductor devices, especially III-V
devices on a Si substrate.

ADVANTAGE - Allows controlled relaxation of mix-matched semiconductor layers.
Provides for a chemical-mechanical planarisation method in conjunction with the
growth of relaxed graded buffers to 100% Ge without a concomitant increase in
threading **dislocation** density. Provides modifications to UHV-CVD procedures
which eliminate surface cracks due to the thermal mismatch between Si and Ge,
and particulate defects due to gas-phase nucleation.

WO 9859365A

CHOSEN-DRAWING: Dwg.3/5

TITLE-TERMS: GRADE GERMANIUM **SILICON** LAYER MISMATCH LAYER **SILICON** SUBSTRATE
ENABLE THREAD DISLOCATE DENSITY CONTROL

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C01;

EPI-CODES: U11-C01J1; U11-C01J8B;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1999-024589
Non-CPI Secondary Accession Numbers: N1999-058603